WHAT IS CLAIMED IS:

1. A method for decreasing CHC degradation, comprising:

providing a semiconductor device having at least one metal layer completed;

applying a planarizing dielectric layer on top of the semiconductor device; and

providing a hydrogen treatment until hydrogen diffuses throughout the semiconductor device.

2. The method of Claim 1, wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen rich environment.

3. The method of Claim 1, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

4. The method of Claim 1, wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

5. The method of Claim 1, wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

6. The method of Claim 1, wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating over a first layer of dielectric material.

7. The method of Claim 1, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD over two layers of dielectric material.

8. The method of Claim 1, wherein the semiconductor device undergoes an N_2 bake after an HSQ layer of a multilayer planarizing dielectric layer is added.

9. The method of Claim 1, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of a multilayer planarizing dielectric layer is added.

10. A semiconductor device for reducing CHC degradation comprising:

a gate oxide region completely saturated with hydrogen formed outwardly from a substrate;

a gate region formed outwardly from the gate oxide region; and

a dielectric layer formed outwardly from the substrate, the gate oxide region and the gate region.

11. The semiconductor device of Claim 10, wherein the gate oxide region, the gate region and the dielectric layer are saturated with hydrogen.

12. A semiconductor device manufactured using the following process:

providing a semiconductor device having at least one metal layer completed;

applying a planarizing dielectric layer on top of the semiconductor device; and

providing a hydrogen treatment until hydrogen diffuses throughout the semiconductor device.

13. The semiconductor device of Claim 12, wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen rich environment.

14. The semiconductor device of Claim 12, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

15. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

16. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

17. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

18. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layers of dielectric material.

19. The semiconductor device of Claim 12, wherein the semiconductor device undergoes an N_2 bake after an HSQ layer of a multilayer planarizing dielectric layer is added.

20. The semiconductor device of Claim 12, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.